Printed circuit board assembly network test optimization

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ABSTRACT

In recent years, due to the impact and changes of the new crown pneumonia epidemic, war and resource management and control on global trade and work patterns, the communication and operation of the past have changed in communication infrastructure, new technology, 5G and Internet e-commerce. The demand for Printed Circuit Board Assemblys related to semiconductors and high-end information and communication products such as servers and 5G base stations has grown more significantly.

The size reduction and weight reduction of semiconductors and high-end information and communication products, the line spacing, line width, board thickness and size of the active and passive components of the printed circuit board will be more dense and reduced due to the above requirements. After the production is completed, the printed circuit board assembly is used in the past functional verification test (FVT) or functional test (FCT) inspection, the test coverage, verification and problem finding and elimination of the network, components and component functions will become the subject of major manufacturers.

Some domestic manufacturers have introduced electrical test (ICT) or manufacturing defect analysis (MDA) and found that the test coverage rate can be effectively improved. When faced with mass production, they need to overcome the problem of long test time. How to reduce the time required for testing and test misjudgment, the risk and loss of circumstances and test omissions are the subject and scope of this

study. This study proposes to optimize the time of the network insulation test of the printed circuit board assembly and reduce the occurrence of test misjudgment by using the frequency node test method.

Keyword: Printed circuit board assembly、Network insulation test、Frequency node test method